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BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			KROFCHECK, MICHAEL C	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/769,201	<b>Applicant(s)</b> ROTITHOR ET AL.	
	<b>Examiner</b> Michael Krofcheck	<b>Art Unit</b> 2186	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 January 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-45 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

1. This office action is in response to application 10/769,201 filed on 1/29/2004.
2. Claims 1-45 have been submitted for examination.
3. Claims 1-45 have been examined.

### ***Drawings***

4. The drawings are objected to because figures 1a, 3a, 4a, and 5a contain text that overlaps with the boxes that are supposed to surround the text, making it difficult to read. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

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the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. Figure 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

6. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

7. The abstract of the disclosure is objected to because it contains the phrase, "has been disclosed." Correction is required. See MPEP § 608.01(b).

8. The disclosure is objected to because of the following informalities: in paragraph 0051 there is a reference to a figure 7. There is no such figure in the drawings or the description of drawings.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for sending a header not contiguously with its respective read data return (shown in figs. 5 and 6 and their explanations), does not reasonably provide enablement for sending the header before the read data return arrives at one of the buffers. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 14-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. Claims 14 and 15 recites the limitation "the header" in line 1 of each claim. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 43-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Dover, US patent application publication 2003/0005239.

16. With respect to claim 43, Dover teaches of a method comprising: checking whether a buffer holds a critical chunk of a cache line of an oldest read return in a queue (fig. 1; paragraph 0014-0017; if the bus is busy transactions are stored in the host response queue (buffer) and if critical data is contained in the queue it is sent once the bus is available. As priority is given in the request queue to the first received data (oldest), the oldest response critical data would be received before the not oldest critical data);

sending the critical chunk if the buffer holds the critical chunk (fig. 1; paragraph 0016-0017; if the bus is busy transactions are stored in the host response queue (buffer) and if critical data is contained in the queue it is sent once the bus is available);

checking whether a predetermined number of non-critical chunks of the cache line have accumulated in the buffer after the critical chunk is sent and sending the non-

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critical chunks if the predetermined number of non-critical chunks have accumulated in the buffer (paragraph 0016-0018; the host interpreter combines responses in to a burst response and stores it in the response queue (buffer). A burst operation has a set, predefined number of chunks that are transmitted with the burst).

17. With respect to claim 44, Dover teaches of removing the oldest read return from the queue after sending the non-critical chunks (fig. 1; paragraph 0014-0015; as the oldest request has been completed it must be removed from the queue or else the queue would become filled with irrelevant requests and have no space for relevant ones).

### ***Claim Rejections - 35 USC § 103***

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

21. Claims 1-3, 5 rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA), Janzen, US patent application publication 2003/0018845, and Dodd et al., US patent application publication 2003/0182513.

22. With respect to claim 1, AAPA teaches of a method comprising: packing a cache line of each of a plurality of read data returns into one or more packets (paragraph 0005);

splitting each of the one or more packets into a plurality of flits (paragraph 0005);

AAPA fails to specifically teach of interleaving the plurality of flits of each of the plurality of read data returns. However, Dodd teaches of interleaving the output of a plurality of read returns (fig. 4-6, paragraph 0026).

Janzen teaches of interleaving the plurality of flits of each a read data return (paragraph 0031, 0033; each word is a flit).

AAPA and Dodd are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the



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art having the teachings of AAPA and Dodd at the time of the invention to interleave the read outputs from multiple memories in AAPA as taught in Dodd. Their motivation would have been to increase the bandwidth efficiency (Dodd paragraph 0026).

The combination of AAPA and Dodd, and Janzen are analogous arts as they are both in the same field of endeavor, accessing memory. It would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Dodd, and Janzen at the time of the invention to interleave the flits of AAPA from the as taught in Janzen. Their motivation would have been to allow the critical word to available first (Janzen, paragraph 0009, 0033).

23. With respect to claim 2, AAPA teaches of comprising sending the flits via a packetized interconnect (paragraph 0005).

24. With respect to claim 3, the combination of AAPA, Dodd and Janzen teach of receiving the plurality of read data returns from a plurality of memory channels in a substantially overlapped manner (Dodd, fig. 5, 8, paragraph 0026; the memory channel runs from each memory device to the controller. As in the combination of AAPA, Dodd and Janzen, the read responses are received with the flits interleaved, and being interleaved between multiple memories, it is abundantly clear to one of ordinary skill in the art that they are received in a substantially overlapped manner).

25. With respect to claim 5, AAPA teaches of adding a header to each of the plurality of read data returns; and sending the header before each of the plurality of read data returns (paragraph 0007; since a header contains information critical to the data in the

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read response, specifically what it is, then it must be sent first, else the controller will not know what is going on).

26. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Dodd, and Janzen as applied to claim 3 above, and further in view of Dover, US patent application publication 2003/0005239.

27. With respect to claim 4, Dover teaches of a queue that prioritizes its entries based on time the request was received (fig. 1; item 135; paragraph 0014-0015).

The combination of AAPA, Dodd, and Janzen and Dover are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Dodd, Janzen, and Dover at the time of the invention to include the queues of Dover in the combination of AAPA, Dodd, and Janzen. Their motivation would have been to allow for the controller to store transactions in the event that the bus or memory is busy, Dover paragraph 0014.

In the combination of AAPA, Dodd, Janzen and Dover, it is abundantly clear to one of ordinary skill in the art that the critical chunk of the oldest request is sent in first flits as the oldest request is sent to the memory first and Janzen teaches of the critical word being sent first. The same can be said for the next oldest request, sent after the first oldest.

28. Additionally, claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA), and Janzen, US patent application publication 2003/0018845.

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29. With respect to claim 1, AAPA teaches of a method comprising: packing a cache line of each of a plurality of read data returns into one or more packets (paragraph 0005);

splitting each of the one or more packets into a plurality of flits (paragraph 0005);

AAPA fails to specifically teach of interleaving the plurality of flits of each of the plurality of read data returns. However, Janzen interleaving the plurality of flits of each of the plurality of read data returns (paragraph 0031, 0033; each word is a flit). This limitation of the claim does not clearly state how the flits are interleaved: if they are interleaved among themselves, or if they are interleaved with flits from the other read data returns.

AAPA and Janzen are analogous arts as they are both in the same field of endeavor, accessing memory. It would have been obvious to one of ordinary skill in the art having the teachings of AAPA, and Janzen at the time of the invention to interleave the flits of AAPA from the as taught in Janzen. Their motivation would have been to allow the critical word to available first (Janzen, paragraph 0009, 0033).

30. Claims 31-42, rejected under 35 U.S.C. 103(a) as being unpatentable over Dover and Dodd.

31. With respect to claim 31, a method comprising: interleaving a plurality of flits containing a critical chunk of each of a first and a second cache lines corresponding to a first and a second read data returns, respectively; sending the interleaved flits (fig. 4; paragraph 0040-0041; each critical word (critical chunk) is a flit. As they are separate responses, each critical word is from a separate cache line);

Dodd teaches of sending a plurality of flits in a group (fig. 4; paragraph 0025-0026; each chunk is a flit).

Dover and Dodd are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Dover and Dodd at the time of the invention to include the sending of the flits of each response in a cluster in the order requested. Their motivation would have been to efficiently utilize the bandwidth (Dodd paragraph 0026). In the combination, since the critical data has been already sent, the remaining data is non-critical data.

32. With respect to claim 32, Dodd teaches of sending a third plurality of flits containing the second cache line's non-critical chunks after the second plurality of flits are sent (fig. 4; paragraph 0025-0026; each chunk is a flit. As the critical data has already been sent in the combination of Dover and Dodd, the remaining data is non-critical).

33. With respect to claim 33, Dover teaches of wherein the first and second read data returns are from a first and a second memory channels, respectively (fig. 2, 4; paragraph 0040-0041; each read response is sensed from a separate sensing device. Therefore each is from a different memory channel. Each channel connects the sensing device to the memory).

34. With respect to claim 34, Dover teaches of receiving the first and the second read data returns in a substantially overlapped manner (fig. 4; paragraph 0040-0041; as

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the responses are time shifted or interleaved, they are received overlapping each other).

35. Claims 35-38 and 39-42 are identical to claims 31-34, except in that they extend the invention from 2 cache lines to 3 and 4 cache lines. As this is a mere duplication of the affected areas and there are no different results, claims 35-42 are rejected on the same grounds.

36. Claim 45 rejected under 35 U.S.C. 103(a) as being unpatentable over Dover and AAPA.

37. With respect to claim 45, AAPA teaches of sending chunks via a packetized interconnect (paragraph 0005, 0007).

Dover and AAPA are analogous arts as they are both in the same field of endeavor, memory addressing. It would have been obvious to one of ordinary skill in the art having the teachings of Dover and AAPA at the time of the invention to include the packetized interconnect to send the data words of Dover as taught in AAPA as it is typically done (AAPA paragraph 0005).

38. Additionally claims 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dover and AAPA. AAPA also teaches of checking whether a predetermined number of non-critical chunks of the cache line have accumulated in the buffer after the critical chunk is sent; and sending the non-critical chunks if the predetermined number of non-critical chunks have accumulated in the buffer (paragraph 0007; where once enough chunks have accumulated in the buffer, they are sent to the

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CPU. As the controller must be able to determine what "enough" is, the number must be predetermined).

39. Dependent claims 44-45 are rejected the same as above.

40. Claims 6, 16-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Dover and Blanchard US patent 5793431.

41. With respect to claim 6, Dover teaches of interleaving a first and second of flits of first and second cache lines, respectively (fig. 4; paragraph 0021, 0040-0042; as the requests are processed at the same time, they must be from separate cache lines).

Dover fails to explicitly teach of a first buffer to temporarily hold a first cache line of a first read data return; a second buffer to temporarily hold a second cache line of a second read data return; and a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of flits of the first and second cache lines, respectively.

However, Blanchard teaches of a first buffer to temporarily hold a first data of a first read data return; a second buffer to temporarily hold a second data of a second read data return (fig. 8; items 16, 18; column 7, lines 45-55); and

a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of data (fig. 8; items 16, 18; column 7, lines 45-55).

Dover and Blanchard are analogous arts as they are both in the same field of endeavor, interleaving data. It would have been obvious to one of ordinary skill in the art having the teachings of Dover and Blanchard at the time of the invention to include the buffers corresponding to each data output and the mux used to interleave the data

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contained within the buffers as taught in Blanchard into the controller of Dover. Their motivation would have been to provide Dover with the hardware to combine multiple separate data streams into a single one (Blanchard abstract).

In the combination of Dover and Blanchard, the buffers correspond to the number of requests for data that the controller can handle at one time, thus each one holds a cache line.

42. With respect to claim 16, Dover teaches of wherein the first and second read data returns arrive from a first memory channel and a second memory channel, respectively, in a substantially overlapped manner (fig. 2; paragraph 0023, 0028; where the response arbiter can send the response data with word granularity in a time sliced manner (i.e. overlapping). The separate responses are sent from the memory unit to the sensing units over separate channels as each sensing unit acts upon its own request).

43. With respect to claims 17 and 18, the combination of Dover and Blanchard teaches of a third and fourth buffer as taught above with respect to the first and second buffer. Dover teaches of handling more than one request simultaneously (paragraph 0015) and the example of figs. 2 and 4 show three requests, which would require three of Blanchard's buffers in the combination of Dover and Blanchard. Dover teaches of handling N requests in parallel (paragraph 0052), it is abundantly clear that this includes four.

44. Claim 7-8, 10-14 rejected under 35 U.S.C. 103(a) as being unpatentable over Dover and Blanchard as applied to claim 6 above, and further in view of AAPA.

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45. With respect to claim 7, AAPA teaches of an interface to output the chunks in two packets (paragraph 0007; packetized interconnect (interface) outputs the chunks for each cache line in their own packet; thus for two cache lines and two requests, there would be two packets).

The combination of Dover and Blanchard and AAPA are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Dover, Blanchard and AAPA at the time of the invention to include the packetized interconnect as taught in AAPA to send the request responses in the combination of Dover and Blanchard as it is typically done (AAPA paragraphs 0005, 0007).

In the combination of Dover, Blanchard, and AAPA, the data outputted would be interleaved as is taught in Dover, cited previously.

46. With respect to claim 8, Dover teaches of time-multiplexing the first and the second pluralities of flits in a plurality of time slots to interleave the first and second pluralities of flits (fig. 4; paragraph 0040-0042; where the words are flits). In the combination of Dover, Blanchard, and AAPA this is done by the multiplexer in Blanchard.

47. With respect to claim 10, Dover teaches of statically time-multiplexes the first and the second pluralities of flits (fig. 4; paragraph 0040-0042; as the words are interleaved in fixed time intervals). In the combination of Dover, Dodd, Blanchard, and AAPA, this would be done by the multiplexer of Blanchard.



48. With respect to claim 11, AAPA teaches of wherein the chunks are sent via a packetized interconnect to a processor (paragraph 0005, 0007). In the combination of Dover and Blanchard and AAPA the data words/flits are interleaved.

49. With respect to claim 12, Dover teaches of wherein a critical chunk of the first read data return is sent in one or more flits of the first plurality of flits and a critical chunk of the second read data return is sent in one or more flits of the second plurality of flits (fig. 4; paragraphs 0040-0042; where the critical data for each response is sent in the first data word (flit) of that response).

50. With respect to claim 13, AAPA teaches of wherein a header is added to each of the first and second cache lines (paragraph 0007).

The combination of Dover and Blanchard and AAPA are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Dover, Blanchard and AAPA at the time of the invention to add a header to each of the responses containing the cache line as taught in AAPA in the combination of Dover and Blanchard as it is typical in a packetized interconnect (AAPA paragraphs 0005, 0007).

51. With respect to claim 14, AAPA teaches of wherein the header is sent after the corresponding read data return starts arriving at one of the first and the second buffers (paragraph 0007).

52. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Dover, Blanchard and AAPA as applied to claim 11 above, and further in view of Osborne, US patent application publication 2003/0093632.

53. With respect to claim 15, the combination of Dover, Blanchard and AAPA fails to explicitly teach of the header is sent before the corresponding read data return starts arriving at one of the first and the second buffers. However, Osborne teaches of the header is sent before the corresponding read data return starts arriving (fig. 6a; paragraph 0050-0051; As the header is sent out from the memory when the read is initiated, therefore it is before the read data is received).

The combination of Dover, Blanchard and AAPA and Osborne are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Dover, Blanchard, AAPA and Osborne at the time of the invention to send the read header before receiving the read results in the combination of of Dover, Blanchard, and AAPA as taught in Osborne. Their motivation would have been to further optimize memory read operations (Osborne, abstract).

54. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Dover, Blanchard, and AAPA as applied to claim 8 above, and further in view of Hollums, US patent application publication 2002/0188905.

55. With respect to claim 9, Hollums teaches of dynamically time-multiplexes the first and the second pluralities of flits (fig. 3d, paragraph 0064-0066).

The combination of Dover, Blanchard, and AAPA and Hollums are analogous arts as they are both in the same field of endeavor, interleaving data. It would have been obvious to one of ordinary skill in the art having the teachings of Dover, Blanchard, AAPA and Hollums at the time of the invention to incorporate the process of dynamically

interleaving the words in the combination of Dover, Blanchard, and AAPA as taught in Hollums. Their motivation would have been to more optimally interleave the data with different interleave depths (Hollums, paragraph 0064-0065).

In the combination of Dover, Blanchard, AAPA, and Hollums, this would be done by the multiplexer of Blanchard.

56. Claims 19, 25-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Dover, Dodd, and Blanchard.

57. With respect to claim 19, Dover teaches of a system comprising: a first plurality of dynamic random access memory ("DRAM") devices (fig. 1, item 150);

a DRAM channel coupled to the first plurality of DRAM devices (fig. 1; item 140);

memory controller coupled to the first DRAM channel (fig. 1; item 120);

interleaving a first and second of flits of first and second cache lines, respectively (fig. 4; paragraph 0021, 0040-0042; as the requests are processed at the same time, they must be from separate cache lines).

Dover fails to explicitly teach of a second plurality of DRAM devices; a second DRAM channel coupled to the second plurality of DRAM devices; the memory controller including a first buffer to temporarily hold a first cache line of a first read data return from the first DRAM channel; a second buffer to temporarily hold a second cache line of a second read data return from the second DRAM channel; and a multiplexer coupled to the first and second buffers to interleave flits of the first and second cache lines.

However, Dodd teaches of a second plurality of DRAM devices (fig. 5, 8; paragraph 0004, 0026);

a second DRAM channel coupled to the second plurality of DRAM devices (fig. 5, 8; paragraph 0026; shown in fig. 5; a channel is connected from each memory to the bus 16)

Blanchard teaches of a first buffer to temporarily hold a first data of a first read data return; a second buffer to temporarily hold a second data of a second read data return (fig. 8; items 16, 18; column 7, lines 45-55); and

a multiplexer coupled to the first and second buffers to interleave a first and a second pluralities of data (fig. 8; items 16, 18; column 7, lines 45-55).

Dover and Dodd are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Dover and Dodd at the time of the invention to include multiple memory devices/ranks and their channels as taught in Dodd into Dover. Their motivation would have been to increase the amount of data that can be stored in the DRAM.

The combination of Dover, and Dodd, and Blanchard are analogous arts as they are both in the same field of endeavor, interleaving data. It would have been obvious to one of ordinary skill in the art having the teachings of Dover, Dodd, and Blanchard at the time of the invention to include the buffers corresponding to each data output and the mux used to interleave the data contained within the buffers as taught in Blanchard into the controller corresponding to each memory in the combination of Dover and Dodd. Their motivation would have been to provide the combination of Dover and Dodd

with the hardware to combine multiple separate data streams into a single one (Blanchard abstract).

In the combination of Dover Dodd, and Blanchard, the buffers correspond to each of the memory devices that the controller is attached to, thus each one holds a cache line from the request to that respective memory.

58. With respect to claim 25, Dover teaches of wherein a critical chunk of each of the first and second read data returns is sent in one or more flits (fig. 4; paragraphs 0040-0042; where the critical data for each response is sent in the first data word (flit) of that response).

59. With respect to claim 26, Dover teaches of wherein the memory controller receives the first and second read data returns in a substantially overlapped manner (fig. 2; paragraph 0023, 0028; where the response arbiter can send the response data with word granularity in a time sliced manner (i.e. overlapping))

60. With respect to claim 27, Dover teaches of further comprising a processor coupled to the memory controller to receive the interleaved flits of the first and second cache lines (fig. 1, items 100, 105; paragraph 0013).

61. With respect to claim 28, Dover teaches of wherein the processor comprises a demultiplexer to separate the flits received (paragraph 0040-0042; As the words (flits) are sent in an interleaved fashion to the host (processor), it is abundantly clear to one of ordinary skill in the art that the host contains a demux to "decode" the words).

62. With respect to claims 29 and 30, the combination of Dover, Dodd, and Blanchard teaches of a third and fourth buffer as taught above with respect to the first

and second buffer. Dodd teaches of additional memory devices (paragraph 0026). Dover teaches of handling more than one request simultaneously (paragraph 0015) and the example of figs. 2 and 4 show three requests. With each memory requiring a buffer from Blanchard in the combination of Dover and Blanchard, four DRAMs would require four buffers. Dover teaches of handling N requests in parallel (paragraph 0052), it is abundantly clear that this includes four.

63. Claim 20-21, 23-24 rejected under 35 U.S.C. 103(a) as being unpatentable over Dover, Dodd, and Blanchard as applied to claim 19 above, and further in view of AAPA.

64. With respect to claim 20, AAPA teaches of an interface to output the chunks in two packets (paragraph 0005, 0007; packetized interconnect outputs the chunks for each cache line in their own packet; thus for two cache lines and two requests, there would be two packets).

The combination of Dover, Dodd, and Blanchard and AAPA are analogous arts as they are both in the same field of endeavor, memory accessing. It would have been obvious to one of ordinary skill in the art having the teachings of Dover, Dodd, Blanchard and AAPA at the time of the invention to include the packetized interconnect as taught in AAPA to send the request responses in the controller of combination of Dover, Dodd, and Blanchard as it is typically done (AAPA paragraphs 0005, 0007).

In the combination of Dover, Dodd, Blanchard, and AAPA, the data outputted would be interleaved as is taught in Dover, cited previously.

65. With respect to claim 21, Dover teaches of time-multiplexing the first and the second pluralities of flits in a plurality of time slots to interleave the first and second

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pluralities of flits (fig. 4; paragraph 0040-0042; where the words are flits). In the combination of Dover, Dodd, Blanchard, and AAPA this is done by the multiplexer in Blanchard.

66. With respect to claim 23, Dover teaches of statically time-multiplexes the first and the second pluralities of flits (fig. 4; paragraph 0040-0042; as the words are interleaved in fixed time intervals). In the combination of Dover, Dodd, Blanchard, and AAPA, this would be done by the multiplexer of Blanchard.

67. With respect to claim 24, AAPA teaches of a packetized interconnect coupled to the memory controller to send the chunks (paragraph 0005, 0007). In the combination of Dover, Dodd, and Blanchard and AAPA the data words/flits are interleaved.

68. Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Dover, Dodd, Blanchard, and AAPA as applied to claim 21 above, and further in view of Hollums.

69. With respect to claim 22, Hollums teaches of dynamically time-multiplexes the first and the second pluralities of flits (fig. 3d, paragraph 0064-0066).

The combination of Dover, Dodd, Blanchard, and AAPA and Hollums are analogous arts as they are both in the same field of endeavor, interleaving data. It would have been obvious to one of ordinary skill in the art having the teachings of Dover, Dodd, Blanchard, AAPA and Hollums at the time of the invention to incorporate the process of dynamically interleaving the words in the combination of Dover, Dodd, Blanchard, and AAPA as taught in Hollums. Their motivation would have been to more

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optimally interleave the data with different interleave depths (Hollums, paragraph 0064-0065).

In the combination of Dover, Dodd, Blanchard, AAPA, and Hollums, this would be done by the multiplexer of Blanchard.

**Conclusion**

70. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

71. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

72. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

73. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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